RESEARCH DEPARTMENT

Switching and storage in line-store standards converters which utilize line-delay interpolation

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THE BRITISH BROADCASTING CORPORATION
ENGINEERING DIVISION

RESEARCH DEPARTMENT

SWITCHING AND STORAGE IN LINE-STORE STANDARDS CONVERTERS WHICH UTILIZE LINE-DELAY INTERPOLATION

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SUMMARY

Problems of switching and storing video signals, which would be encountered in the realization of line-storage standards-conversion, are discussed qualitatively and quantitatively. There follows a description of the development of specimen circuits meeting the requirements defined.

1. INTRODUCTION

1.1. General

Two factors have recently led to increased interest in the possibility of a 'tubeless' standards converter, utilizing only semiconductors and passive components.[1,2] First, the advent of dual-standard operation in the U.K. will necessitate conversion on an unprecendented scale; the improvements in technical quality and in operational convenience likely to result from realization of such a converter would therefore be particularly valuable.

Secondly, recent advances in semiconductor technology have made it possible to envisage relatively cheap circuits that would nevertheless have the requisite performance.

Research Department has accordingly undertaken an investigation into the problems involved in performing some of the essential functions of standards conversion by means of semiconductor devices and passive components. This report is concerned with problems of switching and storage which would be encountered in realizing a practical converter, and includes descriptions of specimen circuits developed in the course of the investigation.

1.2. 'Image-Transfer' and 'Line-Store' Conversion

When a standards converter operates between input and output standards whose field pulses are not synchronized, any interval up to a complete picture period may elapse between the moments at which a given picture element is 'written' at one standard and 'read' at the other. Provision must therefore be made for storing an

entire picture of video information within the converter, which must, in consequence, contain about 200,000 separate storage cells. This number of cells can be made available only by the use of some form of storage surface. In present-day converters, which all use the 'image-transfer' method, storage takes place both on the face of the display tube and on the target of the camera. If, however, two standards having the same nominal field-frequency are rigidly synchronized, so that their field periods are coincident, it can be arranged that each picture element is read out of the converter within the output-line period of being written in, and it is then necessary only to provide storage for one line of video information. The number of storage cells required is thus only five or six hundred (the number of picture elements per line), and it becomes feasible to construct a converter in which the video signal is processed entirely by circuits consisting of separate and accessible components. Such a device, which has been called a 'line-store' converter, would replace 'image-transfer' conversion which, as experience has shown, can impair picture quality to an extent considerably in excess of that inherent in the conversion of scanning standards. Furthermore, a standards converter using only conventional components would be unlikely to need the careful adjustment and constant attention that a skilled operator must provide for an image-transfer converter.

Thus a line-store converter is an attractive device in principle. However, its practicability remains to be established, and this largely depends upon the combination of performance, reliability and cheapness that can be achieved in the basic storage-circuit, which must be replicated more than 500 times. In this report the specification of such a circuit is discussed, and practical investigations that have yielded satisfactory designs are outlined.

2. FUNDAMENTAL PROCESSES OF LINE-STORE STANDARDS-CONVERSION

The storage cells of a line-store converter must be associated with two switching systems; a writing system must direct each picture element of the incoming signal into its correct storage cell and a reading system must subsequently collect the stored picture elements, in the right order, at the times they are required by the outgoing standard.

One means of realizing these systems consists of combining each storage element with a writing switch and a reading switch, as shown in Fig. 1. A common connexion to all the writing switches carries the input signal, and the output signal is generated in a circuit common to all the reading switches. It is convenient to give a name to the group of components that must be uniquely associated with every one of the picture elements along each line of the picture, and such a group will be referred to as a 'store unit'. Besides the storage element and its two switches, each store unit must include circuits that operate the switches at the correct instants.

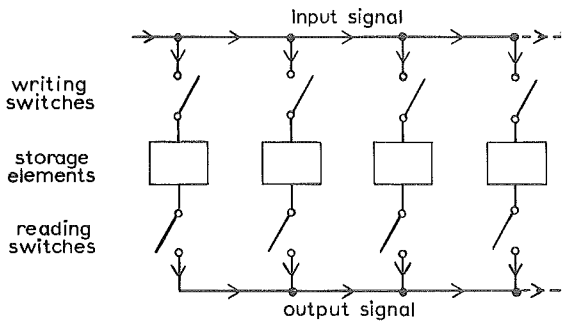

Fig. 1 - Basic operation of line-store standards-converter

In addition to the processes of storage and time-redistribution, a standards converter must also share out the picture information that is carried by the lines of the input standard between the different number of lines of the output standard. This process, in its simplest form, may consist of deriving an output line from a selected input line. However, by an appropriate technique of interpolation, the output line may be synthesized from a suitably weighted sum of two or more consecutive input lines. In a line-store converter, interpolation may be accomplished either by means of a relatively simple circuit within each store unit,[1] or by means of a single but much more complex interpolator external to the store units.[2] Interpolation within each store unit is achieved by utilizing, as the storage element, a low-pass filter which blends together related picture elements fed to it during successive line-periods of the incoming signal. However, when a single interpolator is used, the video signal is processed before being applied to the common input circuit of the store units.* In order to permit addition of signals corresponding to consecutive lines of an input field, these signals must be simultaneously available; an interpolator deriving a signal from two input lines must therefore contain a wide-band delay device capable of delaying the incoming 625-line signal by one line period and is, for this reason, referred to as a 'line-delay' interpolator. Of the 625 lines of the video signal which such an interpolator produces during every picture period, 405 contain, in unconverted form, the information required for the 405 lines of the outgoing signal. It is therefore arranged that the writing switches in the store units operate only during these 405 line-periods, and not during the other 220 line-period with which they are interspersed, when no useful information emerges from the interpolator. By suitably defining an otherwise arbitrary parameter of the interpolator, the designer may select these 220 omitted lines in such a way that, at each store unit, writing and reading always occur alternately.[3]

This mode of operation facilitates the development of an economical store unit in several ways. The separation of the function of interpolation from that of storage allows a single capacitor to serve as the storage element in each unit, and also allows this capacitor to be completely discharged by the reading process; in this way it is possible to achieve an adequate transfer of signal energy from the input circuit to the output circuit without providing power gain in the store unit. Moreover, the alternation of writing and reading operations avoids the simultaneous closure of the two switches in a store unit, which would cause instrumental difficulties.

This report is exclusively concerned with store units designed for use with a line-delay interpolator which utilize a single capacitor as the storage element.

3. BASIC FORMULATION OF THE STORE UNIT

In order that a line of interpolated input signal may be written into a line-store converter, each writing switch in turn must close for an interval approximating to the duration of a picture element; similarly, each reading switch in turn must close during a line-period of the output standard. Such a pattern

*In order to simplify the explanation, it has been assumed throughout this report that conversion is from 625 lines to 405 lines. When conversion involves an increase in the number of lines, it is possible to derive the converter output signal by means of an interpolator fed from the store units.[3] Nevertheless, there are no differences in principle between the two cases, and the distinction is quite irrelevant to the discussion of store units, with which this report is primarily concerned.

of switch operations could be achieved by feeding a line-frequency trigger pulse down a tapped delay line of total delay equal to one line period of the appropriate standard, and supplying successive store units from successive taps on the delay line. The delay line, however, would require a large number of precisely specified components. It has therefore been preferred to employ the logical principle that is used in the 'shift register' of a computer. All the writing switches (say) are supplied with a continuous train of so-called 'clock-pulses' generated by a stable oscillator at the rate of one per picture element, but the switches are designed to close only when a clock pulse coincides with a so-called 'hand-on' pulse generated by closure of the previous switch; in this way a regular progression of switch closures along the line of switches is obtained.

The interconnexions between the store units and the other parts of the converter are as shown in Fig. 2. Each writing or reading circuit, shown in the figure as a single unit, can conveniently be considered as comprising three distinct circuit elements:

a. The Shift Register

This selects the one clock-pulse in each line period that coincides with the hand-on pulse from the previous store-unit.

b. The Switching-pulse Generator

This is triggered by the selected clock pulse and generates a pulse that closes the switch for approximately 100 ns. When suitably delayed, this pulse also serves as the hand-on pulse for the next store unit.

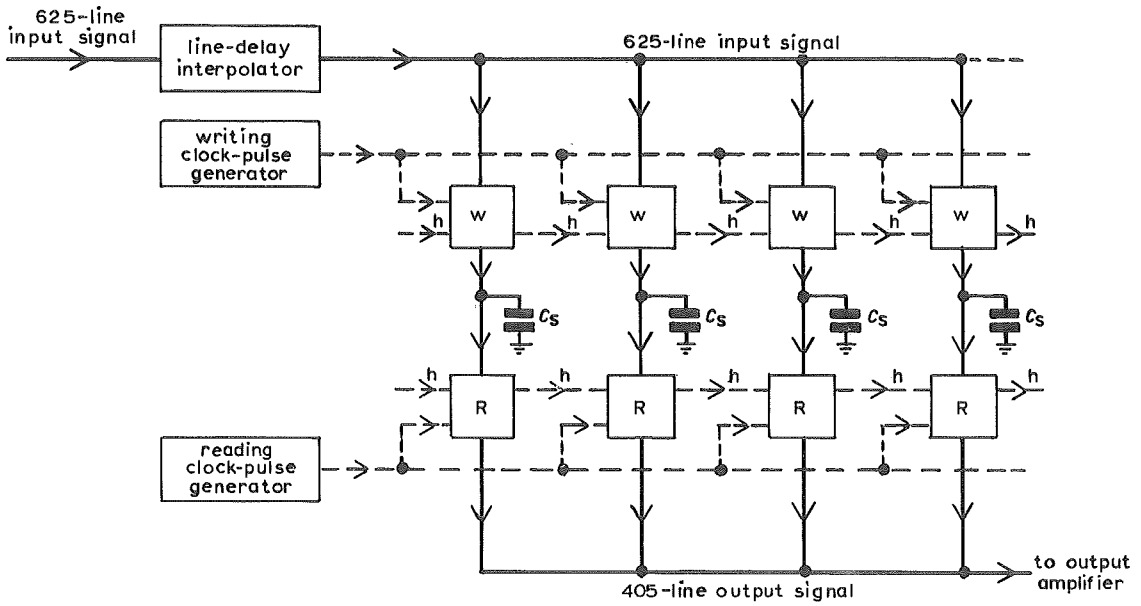

Fig. 2 - Schematic arrangement of store unit

W: Circuits associated with writing
R: Circuits associated with reading
C_s: Storage capacitors
h: Hand-on pulses
——— Signal paths
– – – Pulse paths

c. The Switch

This establishes a conducting path between the store capacitor and the common writing or reading circuit for the duration of the switching pulse and presents a very high-impedance path at all other times.

Of these three elements, only the switch itself handles video signals and it is the design of the switch that presents the most challenging problems. It would, however, be misleading to study this circuit element in isolation; the apparent economy of a particular design might, for instance, be vitiated by the complexity of the switching-pulse generator needed to operate it, while an otherwise satisfactory combination of circuit elements might not allow the economical interconnexion of a large number of store units. The study of switching and storage has, therefore, included all the circuit elements in a store unit and also the means of interconnecting such units.

A prime requirement of a line-store converter, and one that influences almost every aspect of the design of the store units, is that the performance of all store units shall be as similar as possible. Differences of performance cause the picture to be marred by a static 'background' of vertical striations (and tests have been described which establish subjective tolerances for such striations[4]). In order that all the store units should behave similarly they should all encounter the same source impedance at their input terminals and the same terminating impedance at their output terminals. Because the common video-signal connexions of the store units are, of necessity, several feet long, this requirement is most readily met by using tapped transmission lines. The general form of the store unit has now been defined, and the next section deals quantitatively with the design requirements.

4. QUANTITATIVE DESIGN REQUIREMENTS

The very fast operation demanded of the switches in a store unit is the principal factor restricting the choice of semiconductor devices for use as switching elements; 'turn-on' and 'turn-off' times of the order of 5 ns are desirable if full use is to be made of the total available operating period of about 100 ns. Also of great importance, however, are the static characteristics which determine how closely the switch approximates a short circuit when fully 'on' and an open circuit when fully 'off'. The following discussion is concerned with specifying these static characteristics; in this, the lack of emphasis on operating speed is not intended to belittle the paramount importance of that factor.

Some of the switch characteristics can only be specified if the characteristic impedance, Z_0, of the video transmission lines is known, and since satisfactory lines can be made for only a restricted range of impedances, consideration of this parameter forms a suitable starting point for quantitative design. As Z_0 increases, the capacitance presented to each tapping point by the associated store-unit constitutes an increasing proportion of the total capacitance required for the transmission line, and, for practical values of store-unit capacitance, this consideration sets an upper limit of about 55Ω to the value of Z_0.

The lower limit of Z_0 is determined by the techniques used for fabricating the tapped transmission line and by the degree of the non-uniformity of cross-section

which can be tolerated; for example, lines for which Z_0 is less than 5Ω are likely to be non-uniform. These limits of 55Ω and 5Ω are the extremes of practicability; uniform transmission lines having characteristic impedances between 20Ω and 35Ω are relatively easy to provide and an impedance of 25Ω will henceforth be assumed.

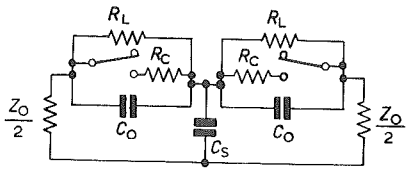

Fig. 3 - Simplified equivalent circuit of the store unit switches

In order to allow approximate values of some of the fundamental parameters of the store unit to be specified, it will be assumed initially that a practical switch can be represented, when closed, by a small series resistance R_c and, when open, by a parallel combination of leakage resistance R_l and shunt capacitance C_0. The basic configuration of the signal path in a complete store unit can then be depicted as in Fig. 3, which shows two switches connecting a storage capacitor C_s to the input and output video transmission lines, respectively; the lines are assumed to have identical characteristic impedances Z_0 and to be correctly terminated at each end, thus presenting impedances of $\frac{1}{2}Z_0$ at both the input and the output of each store unit. In order to establish those values of the parameters shown in the figure that are consistent with satisfactory operation of the store unit, it is necessary to define three basic requirements of performance and make use of the results of subjective tests concerning the threshold visibility of relevant forms of picture impairment.

During each closure of the appropriate switch, the storage capacitor should be charged or discharged substantially to equilibrium. This condition renders the performance of the store unit almost independent of small variations in the charging or discharging time-constant and in the duration of the switching pulse. In order to accommodate the largest variations likely to occur, the store capacitor should be charged to within 1% of the voltage existing on the 'writing' video transmission line; similarly, at least 99% of the charge on the storage capacitor should subsequently be transferred to the 'reading' transmission line. If a closure time of 100 ns is assumed,* these conditions impose a maximum value of 20 ns on the time constants of both the writing and reading circuits. Denoting the total resistance, $R_c + \frac{1}{2}Z_0$, by R_t, we therefore have:

$$C_s R_t < 2 \times 10^{-8} \quad \text{seconds}$$

Once charged, the storage capacitor must not be appreciably discharged by leakage during the storage period, because the magnitude of the discharge due to leakage depends on the storage time, which is not constant. The maximum tolerable rate of discharge is 1% in 100 μs. Since both switches represent leakage paths, this condition imposes the restriction:

$$C_s R_l > 2 \times 10^{-2} \quad \text{seconds}$$

The stray capacitances, C_0, must not couple the two transmission lines sufficiently to cause perceptible contamination of the output signal by unconverted input signal. This requirement imposes the restriction:

$$100 C_0 < C_s$$

*The duration of closure must, in fact, be slightly less than 100 ns for the switches operated by 625-line clock-pulses. This ensures that the disturbance imposed on the transmission line by operation of each switch has passed beyond the next tapping point (towards eventual absorption in the terminating resistance) before the next switch operates.

Thus we have three basic inequalities specifying switch performance:

$$C_s R_t < 2 \times 10^{-8} \quad \text{seconds}$$

$$C_s R_l > 2 \times 10^{-2} \quad \text{seconds}$$

$$100 C_O < C_s$$

These may conveniently be re-arranged and expressed in terms of appropriate practical units:

$$\left.\begin{array}{ll} \text{(i)} & R_t(\Omega) < \dfrac{200}{C_O \text{ (pF)}} \\ \text{(ii)} & R_t(\Omega) < R_l(\text{M}\Omega) \\ \text{(iii)} & \dfrac{2 \times 10^4}{R_t \ (\Omega)} > C_s(\text{pF}) > 100 \text{F}_O \text{ (pF)} \end{array}\right\} \text{where } R_t = R_c + \tfrac{1}{2}Z_O$$

It can be seen from (i) and (ii) that each of the unwanted characteristics of the open switch, C_O and R_l, imposes a maximum value on the total charging or discharging resistance R_t. The inequality (iii) shows that the extent to which the right-hand term of (i) exceeds the left-hand term defines a range of choice for the storage capacitance C_s. The quantities R_c and $\frac{1}{2}Z_O$ are only involved in these expressions in terms of their sum R_t. However, the switch resistance R_c should in fact be as small a fraction of R_t as possible in order that differences between switches shall have the minimum effect on the operation of the store unit.

These inequalities enable a designer to make a quick assessment as to whether or not a semiconductor device of known characteristics merits consideration as a switching element. If, for instance, the shunt capacitance, C_O, of a semiconductor switch is 2·5 pF, then the storage capacitance, C_s, must be at least 250 pF and the value of the switch resistance, R_c, must be considerably less than 80Ω, defined by (i) as a maximum value for R_t. If R_t is assumed to be 80Ω, R_l must be at least 80 MΩ and C_s must be 250 pF. If, however, R_t can be made equal to (say) 20Ω, R_l need only be 20 MΩ and C_s may have any value between 250 pF and 1000 pF.

5. A SPECIMEN DESIGN OF STORE UNIT

5.1. The Switch

So far, the requirements of a switch have been discussed solely in terms of its operating speed, its resistance and shunt capacitance in the non-conducting state, and its resistance in the conducting state. In choosing a practical circuit configuration, however, it is very desirable also that the switch be balanced; that is to say, application of the switching pulse should cause no current to flow in a short circuit joining the switch contacts. This condition demands the use of at least two semiconductor elements that must be closely matched as regards both static and transient characteristics. Use of a balanced switch avoids the need to control precisely the magnitude of the switching pulse because, provided that the pulse is large enough to operate the switch, its magnitude does not affect the output of the store unit.

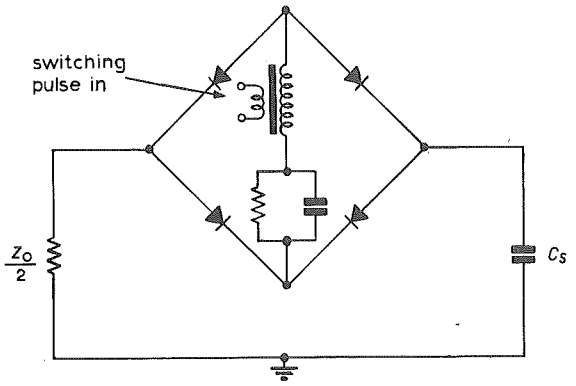

Fig. 4 - Configuration of a practical switch

Various forms of two-, three- and four-layer semiconductor devices may be used as switches; of the possible arrangements that have been investigated, the 4-diode switch shown in Fig. 4 has been found to be the cheapest circuit arrangement capable of meeting all the requirements enumerated. In such a configuration, the values of C_O, R_c and R_l for the bridge of four diodes are the same as for a single diode. For modern diodes with which the required speed of operation can be obtained, a typical value for R_c is 7Ω. As stated earlier, a transmission line can readily be designed to have an impedance of about 25Ω; the total charging or discharge resistance $R_t = R_c + \frac{1}{2}Z_O$ is, therefore, about 20Ω. Thus the inequalities derived in the preceding section require that C_O shall be less than 10 pF and R_l shall be greater than 20 MΩ. This last figure precludes the use of fast germanium diodes, but the available range of fast silicon diodes includes several types which meet the above requirements.

One of the best of these is the IN916 diode for which $R_c = 7\Omega$, $C_O = 2$pF and $R_l = 750$ MΩ. Diodes specified by this type-number are marketed by a number of manufacturers, at a typical unit cost of 6s. 6d., (and it is possible that this price may be reduced by about a third within the next year).

When experimental switches were constructed using diodes of this type it was found that although the other conditions enumerated were easily met, an excessive degree of unbalance occurred in bridges made up at random from a batch of diodes. Lack of balance results in a constant error between the input and output signals of the store unit and is one of the factors producing striations in the converted picture. Some improvement in the ratio of video signal to added component can be made by using a larger video signal. However, this necessitates increasing the switching current with consequent aggravation of the unbalance, and it has been found in practice that little is gained by using a video level of more than 6 V, peak to peak.

The unbalance of a complete store unit is conveniently measured by connecting the unit between resistive terminations of $\frac{1}{2}Z_O$, operating writing and reading switches alternately, and observing the step, ΔV_s, in the voltage across the storage capacitor caused by each operation of the reading switch. This step signifies a transfer of charge to the reading circuit of the same magnitude as that which would result from application of a video voltage ΔV_s to a perfectly balanced store unit.

Experiments have shown that this unbalance is primarily a high-frequency phenomenon produced by differences in the hole-storage and 'forward recovery-time' characteristic of the diodes, and despite the use of diodes that are, individually, satisfactory in these respects, it has, nevertheless, been found necessary to employ a process of selection in order to bring the unwanted added signal below the level corresponding to the threshold of perceptibility for vertical striations.

Two methods of selection have been used successfully. In the first method, selection is applied to groups of four diodes; these groups each contain diodes

having similar characteristics at low frequencies, and are supplied by the manufacturers as 'matched quads'. Each quad is incorporated in a high-speed switch circuit similar to that used in the complete store unit and is classified according to the direct voltage, ΔV, appearing across the storage capacitor as a result of repeated operation of the switch. Store units are then made up, the writing switch and the reading switch of each unit consisting of quads 'paired' for similar values of ΔV; by connecting the two quads appropriately substantial cancellation of unbalance is achieved.

The second method of selection, which applies to single diodes, again involves determining the out-of-balance voltage, ΔV, for a high-speed switch. In this method, three arms of the bridge contain diodes previously selected for identical characteristics, and the diodes from an incoming batch are, in turn, inserted in the fourth arm; each diode can thus be classified by a value of ΔV. Quads are then made up, each from a group of four diodes yielding similar values of ΔV. By this means diodes are matched sufficiently well for pairing of the resultant quads to be unnecessary.

When diodes chosen at random are assembled into quads, which are then used without 'pairing', the total unbalance of a store unit, ΔV_s, is typically $\pm$ 200 mV. This figure can be reduced to about $\pm$ 60 mV by the use of unpaired quads whose individual diodes have been matched for low-frequency characteristics alone, and to about $\pm$ 10 mV by either of the two selection procedures described above.

So far, the effects of circuit inductance have been disregarded, but, at the switching speeds under discussion, inductance has, in fact, a significant effect upon the charging and discharging of the storage capacitor. In a practical layout involving a transmission line and a printed-circuit board the total length of the charging or discharging path is at least two or three inches, the inductance of which is about 0·1 μH.

A simplified equivalent circuit which includes a stray inductance L_0 is shown in Fig. 5(a).

The transient voltage waveforms after closure of the switch have been calculated for four typical values of inductance and are shown in Fig. 5(b); it has been assumed that the applied voltage step is positive-going and that the circuit has C_s = 400 pF and $R_t = R_c + \frac{1}{2}Z_0 = 20\Omega$.

The requirement is that the voltage across C_s should rise rapidly to within, say, $\pm$ 1% of the applied voltage and then remain within these limits. Fulfilment of this condition ensures that the stored charge is almost unaffected by small variations in the values of L_0 or R_t, or in the duration of switch closure; the charge is, in fact, related almost exclusively to the applied voltage by the value of C_s, which can be controlled within a very close tolerance and should remain stable with changes of temperature over a long period of time.

From Fig. 5(b) it can be seen that the voltage across C_s remains within 1% of the applied voltage after 36 ns in a circuit with no inductance, after 26 ns for L_0 = 0·04 μH and after 32 ns for L_0 = 0·064 μH. For values of L_0 up to 0·08 μH the charging of the capacitor to within 1% of the applied voltage is more rapid

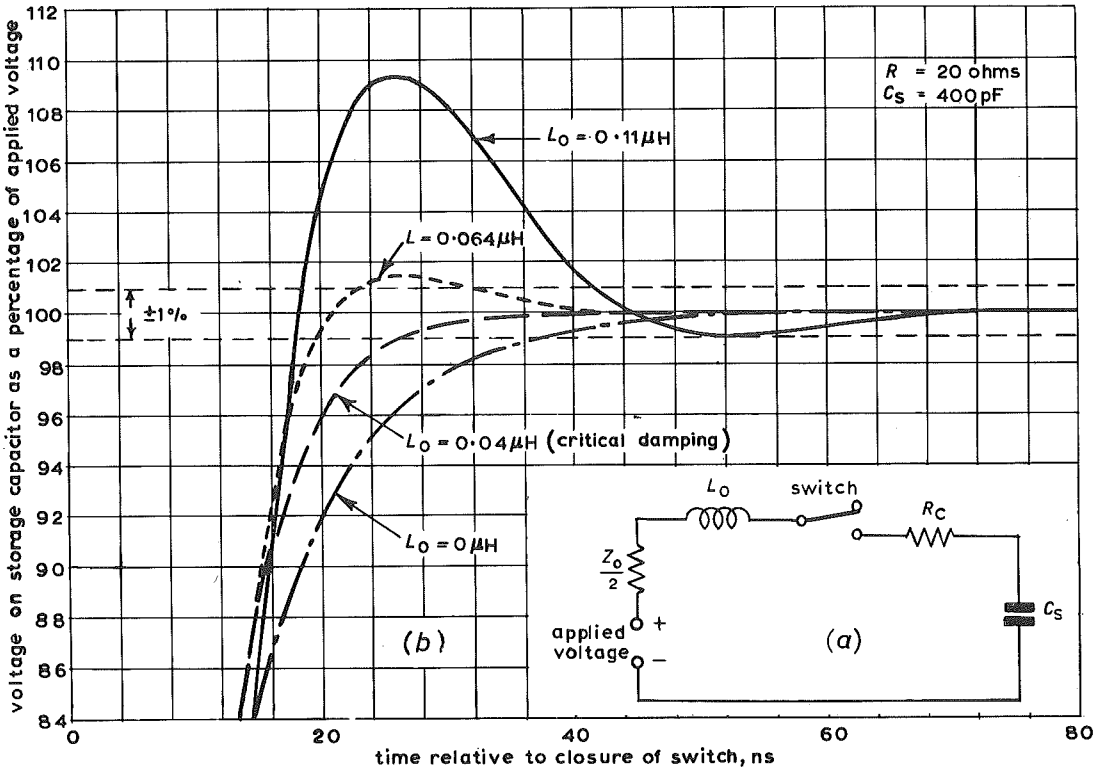

Fig. 5 - The effect of circuit inductance on the charging process

(a) Equivalent circuit including inductance L_O
(b) Voltage waveform across C_s for four values of L_O

than for R_t and C_s alone and the stray circuit inductance becomes a useful adjunct rather than an embarrassment. Above 0·08 μH the presence of inductance extends the time for which the voltage across C_s differs by more than ± 1% from the applied voltage, and, for 0·11 μH, Fig. 5(b) shows this time to be 42 ns. Thus it is important to reduce the circuit path length to the point where the value of L_O is of the order of 0·04 μH to 0·08 μH.

5.2. The Switching-Pulse Generator and Shift Register

As stated in the previous section, unbalance in the four-diode switches adds an interfering signal to the output of the converter and the video signal must, therefore, be sufficiently large for this interference to be subjectively imperceptible. The required ratio has been shown[4] to be 49 dB, so that the existence of a typical degree of unbalance, equivalent to a spurious input signal of ± 10 mV, necessitates a video-signal magnitude at the writing transmission line of ± 3 V pk.

To charge or discharge a 400 pF storage capacitor through 3 V* within, say, 40 ns demands a mean current of 30 mA. The value of peak current depends upon the circuit inductance and upon the forward recovery-characteristics of the diodes;

*Although the stored potential has a total range of 6 V, it is never changed by more than 3 V at a time, because the store capacitor is discharged to zero potential, by the reading operation, between successive writing operations.

nevertheless, it is at least twice that of the mean current. The peak current supplied by the switching-pulse generator must exceed the peak charging or discharging current by a sufficient margin to maintain good conduction in the diodes and the design should include a margin of safety in order to allow for component tolerances and ageing effects. A peak switching current of 100 mA has therefore been taken as the design figure for the switching-pulse generator.

The use of an unnecessarily large switching current is disadvantageous because spurious signals are thereby increased and because more power is required.

As has already been stated in the discussion of the switch design, the practice of charging and discharging the store condenser to the equilibrium value, and the use of a balanced switch circuit allow the switching-pulse generator to be designed to a specification permitting reasonably wide variations of pulse magnitude and duration, with a consequent saving in cost. The pulse of current through the diodes need be specified to no greater precision than is shown, in Fig. 6, by the area inside the solid lines; the duration must have a value between 60 ns and 100 ns, the maximum current should be maintained for as long as possible and the waveform must be free from significant overshoots. The dotted line in Fig. 6 represents a typical pulse shape.

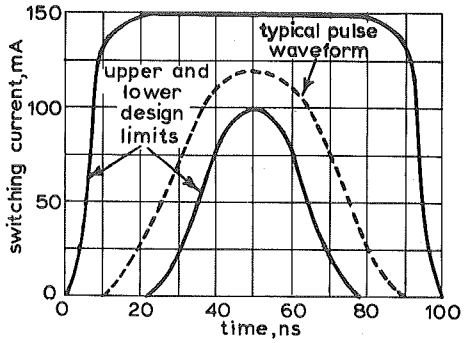

Fig. 6 - Design tolerances for the switching pulse

The circuit used for the switching-pulse generator must, therefore, be the simplest circuit capable of delivering a high-current pulse, of short duration and low duty-factor, with short rise-and-fall times. Two basic configurations potentially capable of meeting these requirements are the blocking oscillator and the avalanche pulse generator; circuits of both forms have been tested, using a number of types of switching transistor. It has been concluded that, while usable circuits can be evolved from either configuration, neither is wholly satisfactory. Fast transients and high currents may be obtained with a blocking oscillator, but the magnitude and shape of the pulse produced by such a circuit is very dependent upon individual semiconductors and transformers. Generators using transistors in the avalanche mode are more consistent, but are sensitive to the magnitude of the triggering pulse and, in general, require a more expensive type of transistor. It has been found possible, however, to combine the advantages of both circuit configurations by applying positive feedback to an avalanche circuit, thereby removing its sensitivity to trigger pulse magnitude. Fig. 7(a) shows the circuit of a complete store unit incorporating an avalanche pulse generator of this type. It will be seen that the feedback is derived by adding a tertiary winding to the transformer that is used in order to couple the unbalanced pulse generator to the balanced load presented by the switch; thus little extra cost is involved.

Fig. 7(a) also shows the way in which the switching-pulse generators in adjacent stores are coupled together in order to provide a 'shift register' as discussed earlier in this report. The condition that each generator shall operate only when it simultaneously receives a clock pulse and a 'hand-on' pulse from the previous store unit is met by interposing an 'and' gate between the clock-pulse

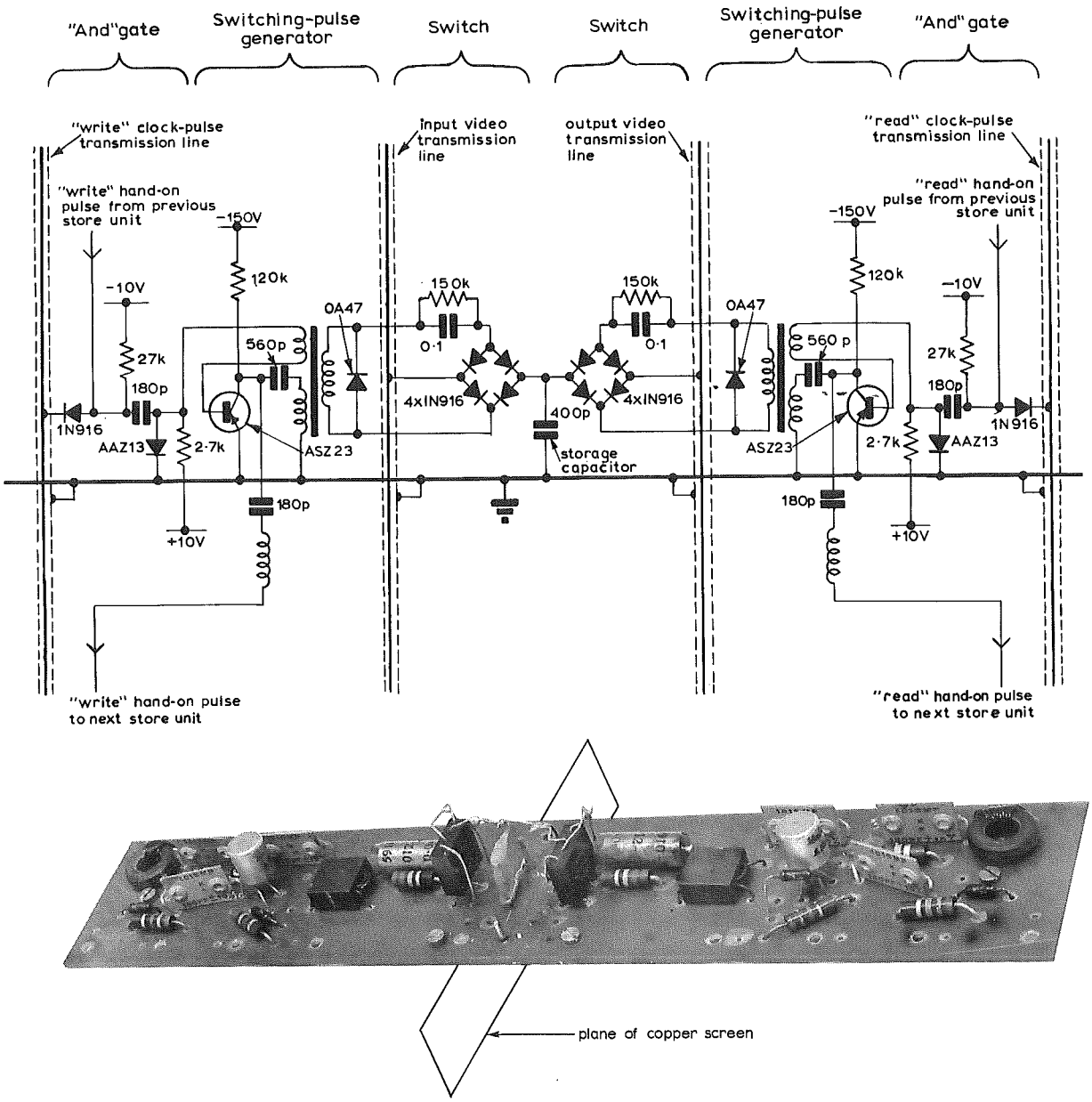

Fig. 7 - A specimen design of store unit

(a) Circuit diagram
(b) Store unit built on a printed-circuit board

input and the trigger circuit of the pulse generator. The hand-on pulse is, of course, initiated by the clock pulse immediately preceding the one with which it must coincide. Delay must, therefore, be incorporated in the coupling between adjacent store-units, and this is accomplished by means of the inductors L_d shown in the diagram. The inductance L_d and the associated stray capacitance at the input to the avalanche pulse generator form a simple delay section.

The appearance of the circuit when embodied in a printed-board assembly is shown in Fig. 7(b); in order to allow the components to be seen more clearly, a small copper screen, usually mounted across the centre of the board, has been removed.

5.3. Assessment of Performance

As has already been stated, mutual capacitance coupling the input and output transmission lines causes contamination of the output signal by unconverted input signal. It has been found[5] that perceptible degradation is avoided if the capacitance is of a lower value than that corresponding to a signal-to-interference ratio of 16 dB at 3 Mc/s. It can be shown that when due allowance is made for the fact that the output signal is of lower magnitude than the input signal, the critical value of the total mutual capacity is 10 pF. Assuming 500 store units, therefore, the capacitance between the input and output of each must be less than 0·02 pF. Measurements, by means of conventional bridge techniques, have established that this condition is in fact fulfilled by the assembly shown in Fig. 7(b), when the copper screen mentioned above is fitted.

In order to allow the remaining aspects of performance to be rapidly assessed, a special testing jig has been constructed, and its operation is illustrated in Fig. 8(a). The store unit under test is subjected to a repetitive cycle of writing and reading, in which each writing operation is followed by four successive reading operations; the period of the whole cycle is equal to four line periods of the 405-line standard. The writing and reading transmission lines are simulated by terminating resistors of value $\frac{1}{2}Z_0$, and a direct voltage of magnitude V and (say) negative polarity is applied in series with the resistor on the input side of the store unit. It is arranged that the shift-register circuits are inhibited, so that all triggering pulses operate the appropriate switching circuits.

As has already been discussed, one of the requirements of a store unit is that the storage capacitor be charged or discharged almost to equilibrium by a single operation of the appropriate switching circuit. If, therefore, an ideal store unit were connected to the testing rig the first reading pulse to follow each writing pulse would result in complete discharge of the storage capacitor, whose voltage would then remain at zero until the next writing pulse caused it to fall to $-V$. The waveform observed on an oscilloscope connected to the storage capacitor would therefore be as shown at the bottom of the diagram. If, however, the reading circuits in the store unit were unable to discharge the capacitor in one operation, a further discharge would take place at the time of the second reading pulse to follow each writing pulse and a positive step would occur in the oscillogram. Furthermore, if the writing switch were of inadequate impedance in its 'off' condition, the storage capacitor would re-charge appreciably towards $-V$ during the intervals between pulses, and positive steps would also occur at the times of the third and fourth reading pulses. By reversing the connexions to the writing and reading sides of the unit, and repeating the test, the charging efficacy of the writing circuits and the leakage of the 'read' switch can similarly be assessed.

Fig. 8(b) shows part of the storage-capacitor waveform for a typical store-unit; the deflexion sensitivity of the oscilloscope used was such that the applied voltage of -3 V corresponded to 300 of the small divisions on the graticule. It may therefore be seen, from the step which occurs at the time of the second reading pulse, that the residual charge left on the storage capacitor after the first reading pulse was only about 0·3% of that stored by the writing process. Moreover, the absence of perceptible steps at the times of the third and fourth reading pulses shows that the effects of leakage were quite negligible.

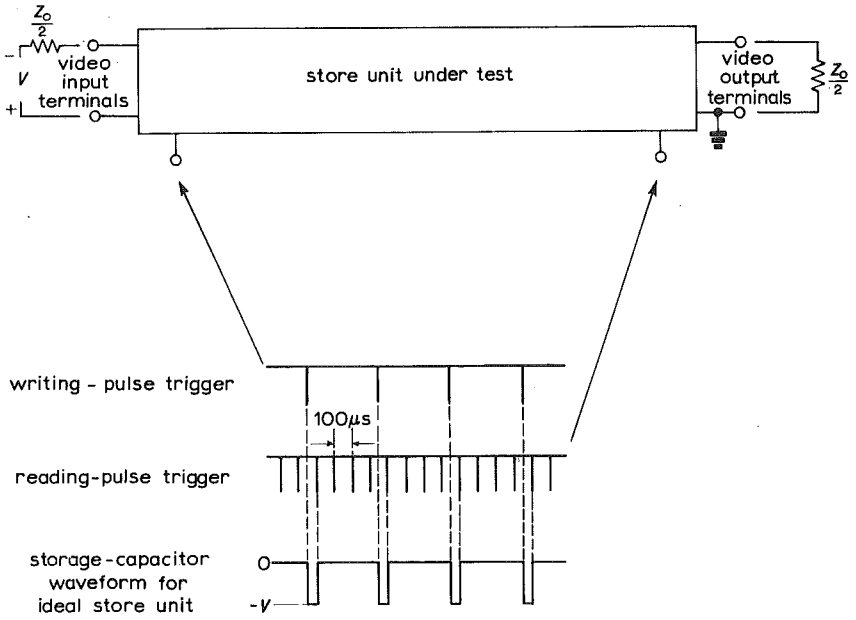

Fig. 8(a) - Testing arrangements for store units

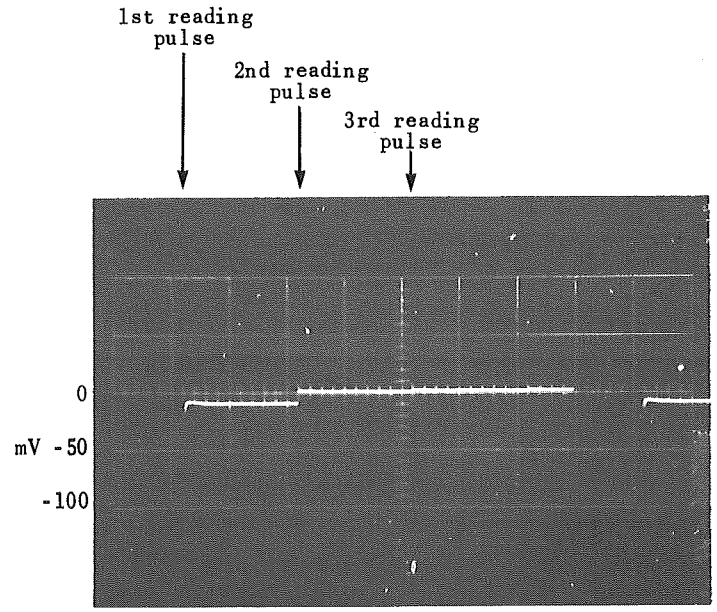

Fig. 8(b) - Waveform on storage capacitor under test conditions

In order to provide an indication of their performance, when incorporated in a line-store converter, 80 store units of the type shown in Figs. 7(a) and 7(b) were constructed using small-scale production techniques. These store units were suitably mounted and connected to video amplifiers and clock-pulse generators by means of tapped transmission lines. Fig. 9 shows photographs of two vertical strips of a 625-line Test Card 'C' converted to the 405-line standard by this assembly; it should be noted that no interpolation was used. The photographs show that the performance of the store units was satisfactory.

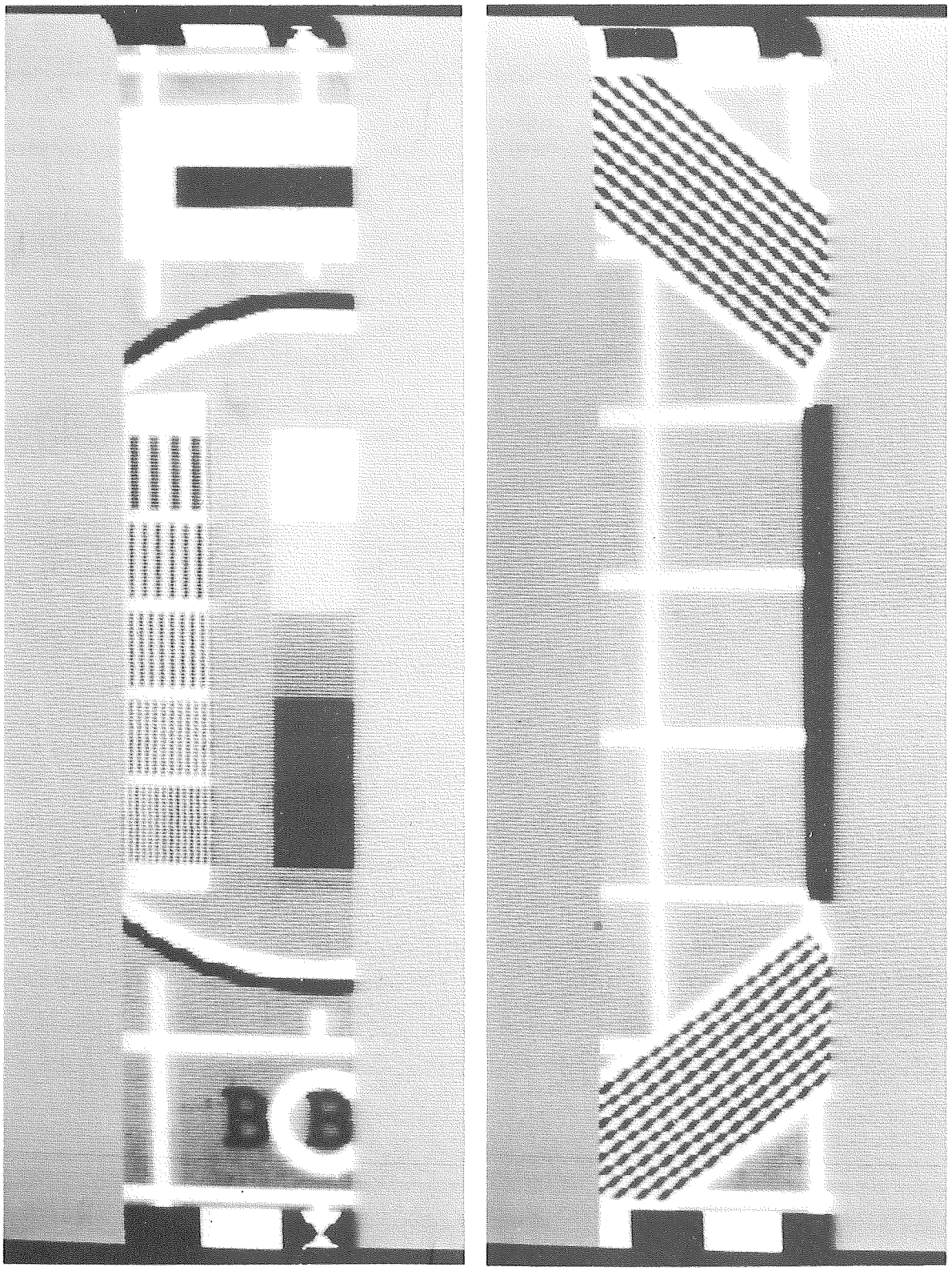

Fig. 9 - Sections of a Test Card 'C' converted, without interpolation from 625 to 405 lines by an experimental assembly of 80 store-units

6. CONCLUSIONS

As a result of the investigation outlined in this report, it has been established that satisfactory store units can be designed without recourse to elaborate circuits or unduly expensive components. Moreover, the writers do not consider that the combination of several hundred store units to form the nucleus of a practical converter would present any serious difficulties.

7. REFERENCES

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